Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CLEAR**
2. **Q1**
3. **N. Q1**
4. **D1**
5. **D2**
6. **N. Q2**
7. **Q2**
8. **GND**
9. **CLOCK**
10. **Q3**
11. **N. Q3**
12. **D3**
13. **D4**
14. **N. Q4**
15. **Q4**
16. **VCC**

**1 16**

**15**

**14**

**13**

**12**

**11**

**10**

**2**

**3**

**4**

**5**

**6**

**7**

**8 9**

**MASK**

**REF**

**.047”**

**.068”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .047” X .068” DATE: 8/29/22**

**MFG: FAIRCHILD THICKNESS .015” P/N: 54LS175**

**DG 10.1.2**

#### Rev B, 7/1